

Chapter 2

Dual-Branch RF Amplifier Design and Architectures

2.1 Introduction

The previous chapter presents the conceptual understanding of power amplifier (PA) design as well as various design considerations and parameters. In the previously presented single-branch amplifiers, efficiency is maximal only at peak power drive, and drops rapidly as soon as the instantaneous input power is decreased. Accordingly, all single-branch PAs, regardless of their classes of operation, will fail to maintain satisfactory efficiency performance when driven with envelope varying wireless communication signals, owing to the high peak-to-average power ratio (PAPR) values of these signals. This stimulated the need for more appropriate alternatives. With the demand for highly efficient communication systems, the need for efficient PAs has increased considerably.

In this chapter, we provide a detailed analysis of the most common dual-branch-based radio frequency (RF) amplifiers with the aim of increasing the output power, power efficiency or the linearity of such amplifiers. These include balanced amplifiers, push–pull amplifiers, Doherty amplifiers, linear amplification with nonlinear components (LINC) amplifiers, and pulsed-load-modulated (PLM) amplifiers. The motivation of using two branches in such amplifiers is to have a combination of two single-ended amplifiers (belonging to the same class or different classes) working in parallel, resulting in higher efficiency and output power or linearity. Different design metrics will be used to evaluate the performance of the various dual-branch topologies, which will indicate significant improvement over their single-branch counterparts in terms of frequency response flatness, insertion loss, output power, power efficiency and linearity. An important step in the design of dual-branch amplifiers is the design of the input splitting couplers/signal separators and output combiners used to split the input signal and connect the output of the individual PAs to form a single output. A lossy or less efficient coupler or combiner will result in a reduced efficiency of the overall system.

2.2 Balanced Amplifiers

The motivation for two-branch balanced amplifiers (BAs) is to increase the 3 dB output power while exhibiting flatter frequency response and better return loss. In addition to increasing the output power, BA topology results in 3 dB higher OIP₃, in comparison to the OIP₃ of the branch amplifier. A typical two-branch BA topology is shown in Fig. 2.1. It consists of a 3 dB quadrature hybrid coupler shown in Fig. 2.2 used to split the input signal into two components with a 90° phase difference between them. The signals are then fed to two paired amplifiers and then combined together by another 3 dB quadrature hybrid coupler at the output of the PAs. Ideally, this results in the same gain and twice the output power as the input signal.

The S matrix of a 4-port hybrid coupler is:

$$S_{90}^Q = \frac{1}{\sqrt{2}} \begin{bmatrix} 0 & 0 & -j & 1 \\ 0 & 0 & 1 & -j \\ -j & 1 & 0 & 0 \\ 1 & -j & 0 & 0 \end{bmatrix}$$

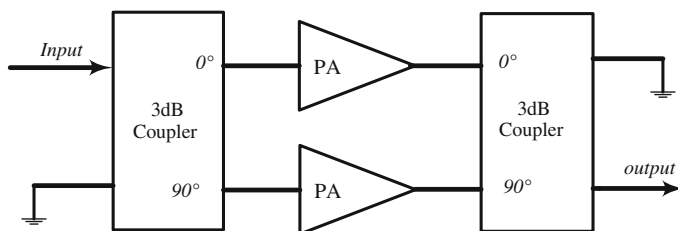
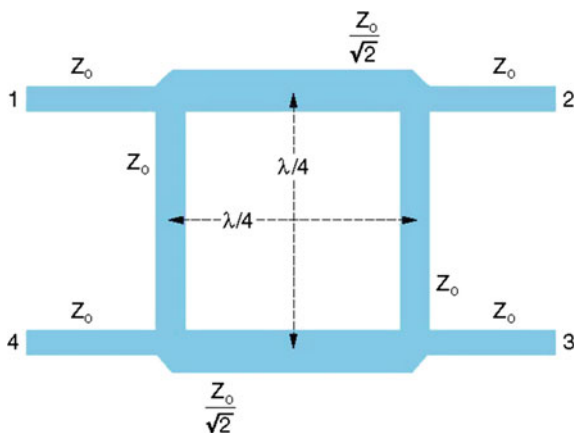


Fig. 2.1 Block diagram of a typical balanced amplifier

Fig. 2.2 Branch line hybrid coupler



The S parameters of the BA can be deduced from those of the PA using the following expressions:

$$S_{11}^{\text{BA}} = -\frac{1}{2}(S_{11}^{\text{A}} - S_{11}^{\text{B}}) \quad (2.1a)$$

$$S_{22}^{\text{BA}} = -\frac{1}{2}(S_{22}^{\text{A}} - S_{22}^{\text{B}}) \quad (2.1b)$$

$$S_{21}^{\text{BA}} = -\frac{j}{2}(S_{21}^{\text{A}} + S_{21}^{\text{B}}) \quad (2.1c)$$

$$S_{12}^{\text{BA}} = -\frac{j}{2}(S_{12}^{\text{A}} + S_{12}^{\text{B}}) \quad (2.1d)$$

It is obvious from the above equations that if amplifier A is identical to amplifier B, and the hybrid couplers are ideal, the resulting S parameters will be:

$$S_{11}^{\text{BA}} = S_{22}^{\text{BA}} = 0 \quad (2.2a)$$

$$S_{21}^{\text{BA}} = -jS_{21}^{\text{A}} \quad (2.2b)$$

$$S_{12}^{\text{BA}} = -jS_{12}^{\text{A}} \quad (2.2c)$$

From the above equations, it can be obviously concluded that the balanced amplifier will have perfect return loss, the same power gain as that of the branch amplifier and twice the output power. P_{1dB} , P_{sat} , and OIP_3 of the balanced amplifier are twice those of the branch amplifier.

The concept of balanced amplifier can be generalized to N balanced amplifiers, and the input and output couplers have to be designed such that they can equally split the input signal in N portions with incremental phase increase of π/N between the branches. The input signal to the amplifier of i th branch should be equal to

$$V_{\text{in}}^i = \frac{V_{\text{in}}}{\sqrt{N}} e^{j\frac{(i-1)\pi}{N}} \quad \text{with } i = 1, 2, \dots, N \quad (2.3a)$$

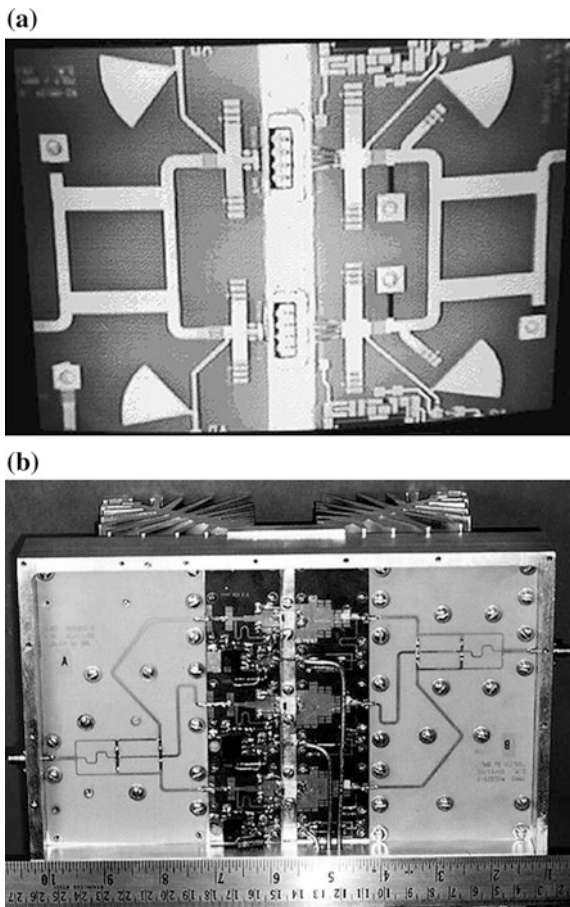
and the output signal power to the amplifier of i th branch should be

$$V_{\text{out}}^i = \frac{S_{21}^i V_{\text{in}}}{\sqrt{N}} e^{j\frac{(i-1)\pi}{N}} \quad (2.3b)$$

In such a case, the S parameters of the identical N -branch balanced amplifier can be written as

$$S_{11}^{\text{BA}-N} = S_{22}^{\text{BA}-N} = 0 \quad (2.5a)$$

Fig. 2.3 Examples of balanced amplifiers: **a** two-branch balanced amplifier and **b** three-branch balanced amplifier



$$S_{21}^{BA-N} = -e^{j\frac{\pi}{N}} S_{21} \quad (2.5b)$$

$$S_{12}^{BA-N} = -e^{j\frac{\pi}{N}} S_{12} \quad (2.5c)$$

Design examples of two- and three-branch balanced amplifiers are shown in Fig. 2.3.

2.3 Push–Pull Amplifiers

Similar to the balanced amplifier topology, the push–pull amplifiers use two class-B amplifiers connected using two H-type (180°) hybrid couplers as shown in Fig. 2.4. The rat-race coupler is the H-coupler and is illustrated in Fig. 2.5. The topology

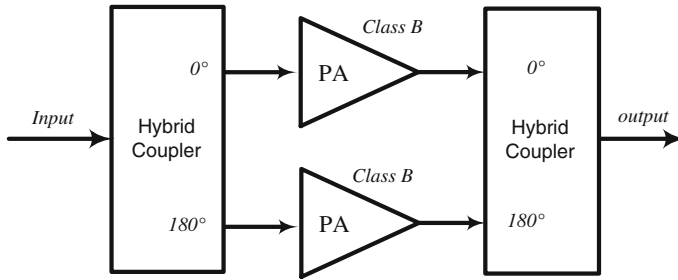
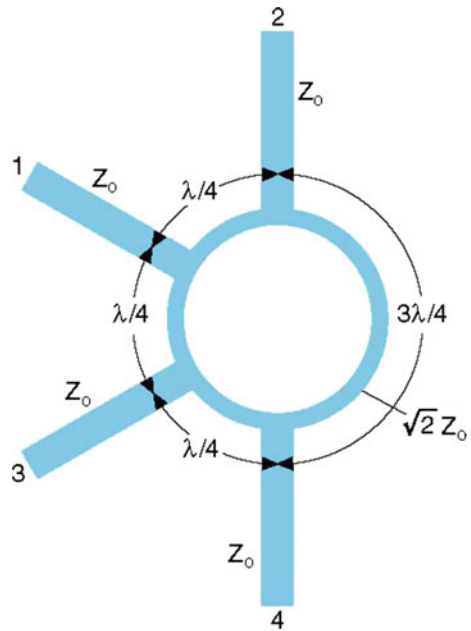


Fig. 2.4 Block diagram of the push-pull amplifier

Fig. 2.5 A rat-race H-coupler



doubles the output power of the branch amplifier while rejecting even order intermodulation distortions, leading to high linearity (despite the use of class-B amplifiers) and reasonable frequency response.

The S -parameter of the rat-race hybrid coupler is

$$S_{180}^H = \frac{-j}{\sqrt{2}} \begin{bmatrix} 0 & 1 & 1 & 0 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & -1 \\ 1 & 0 & -1 & 0 \end{bmatrix} \quad (2.6)$$

2.3.1 Push–Pull Amplifier with Bipolar Transistors

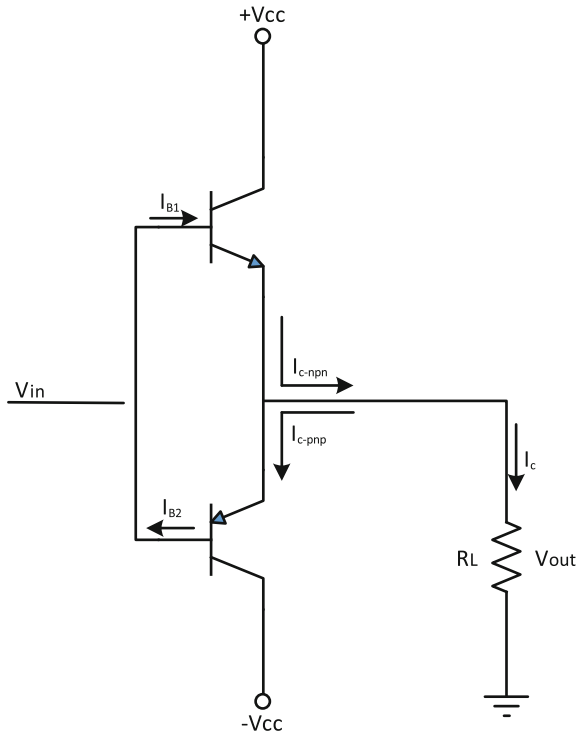
The basic circuit diagram of a balanced amplifier using NPN and PNP bipolar transistors is shown in Fig. 2.6. Here, the NPN and PNP transistors are working in push–pull configuration. Both NPN and PNP transistors are biased in class B but operate in the alternative half cycle of an input sinusoid. Thus, the current drawn from the direct current (DC) power supply by the NPN and PNP transistors are rectified alternative half-sine wave. Based on Eq. (1.55), the currents due to the two transistors are given by

$$I_{c-npn}(t) = I_{\max} \left[\frac{1}{\pi} + \frac{1}{2} \sin(\omega t) - \frac{2}{\pi} \left(\frac{\cos(2\omega t)}{1 \times 3} + \frac{\cos(4\omega t)}{3 \times 5} + \frac{\cos(6\omega t)}{5 \times 7} + \dots \right) \right] \quad (2.7a)$$

$$I_{c-pnp}(t) = -I_{\max} \left[\frac{1}{\pi} + \frac{1}{2} \sin(\omega t - \pi) - \frac{2}{\pi} \left(\frac{\cos(2\omega t - \pi)}{1 \times 3} + \frac{\cos(4\omega t - \pi)}{3 \times 5} + \frac{\cos(6\omega t - \pi)}{5 \times 7} + \dots \right) \right] \quad (2.7b)$$

The addition of the above two current waveforms leads to a pure current sine wave across the output resistance and cancels all even order harmonics. Therefore, in principle, a push–pull amplifier is a linear amplifier. One example of a microwave

Fig. 2.6 Circuit-level implementation of an NPN and PNP push–pull amplifier



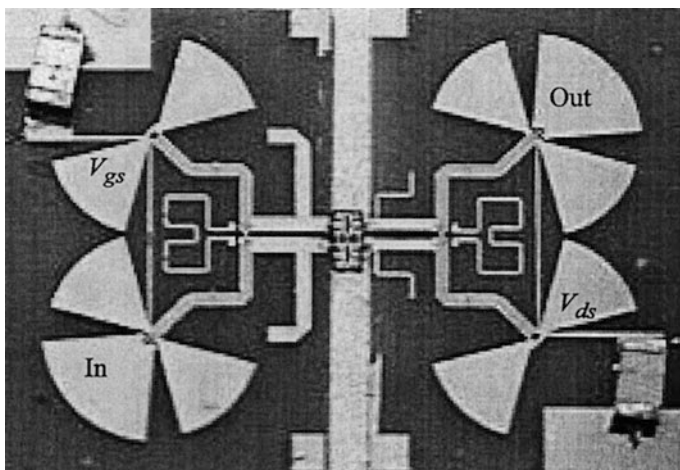


Fig. 2.7 Photograph of a fabricated push–pull microwave power amplifier

power amplifier implementation using the push–pull amplifier configuration is shown in Fig. 2.7.

2.3.2 Push–Pull Amplifier with Baluns

Another topology of push–pull amplifiers requires a three-port balun (balanced–unbalanced) transformation instead of hybrid couplers for splitting and combining of the signals at the input and output of the amplifiers. The purpose of the balun is to transform the unbalanced input signal to balanced signals before being fed to the PAs. Baluns can be implemented as transformers or transmission lines. A transformer-type balun-based push–pull configuration is shown in Fig. 2.8.

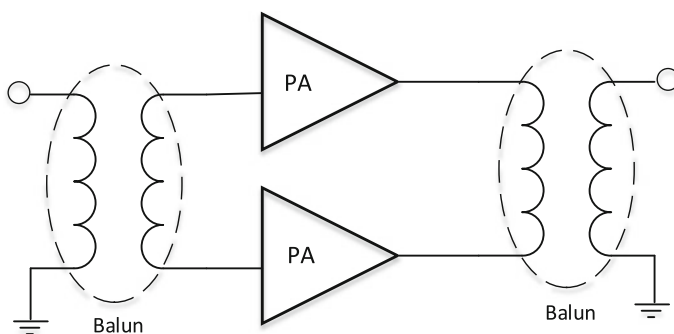


Fig. 2.8 Transformer-type balun-based implementation of a push–pull amplifier

2.4 Doherty Amplifiers

2.4.1 Doherty Amplifier Architecture

The circuit diagram of a Doherty PA is presented in Fig. 2.9. It encompasses two parallel amplifiers, namely, the carrier amplifier (operating in class AB) and the peaking amplifier (operating in class C), an input analog splitter, and a nonisolated output power combiner that consists of two transmission lines, with an electrical length of 90° . In Fig. 2.9, the transmission line connected to the output load, Z_0 , is commonly denominated as an impedance transformer, whereas that having a characteristic impedance of Z_0 is designated as an impedance inverter. Typically, the carrier and peaking amplifiers have identical device sizes and matching networks and are evenly driven. The gate bias of the peaking PA is chosen to control its turn-on region. This defines the Doherty design parameter α ($0 \leq \alpha \leq 1$), which expresses the relative contribution, at full drive, of the carrier amplifier to the total output power of the Doherty PA.

Figure 2.10 shows the equivalent circuit diagram and the ideal output current profile model that are commonly considered for studying the operation of Doherty PAs. The operation of the circuit can be analyzed in two modes: at low-power mode, where only the carrier amplifier is active, and at high power mode, where

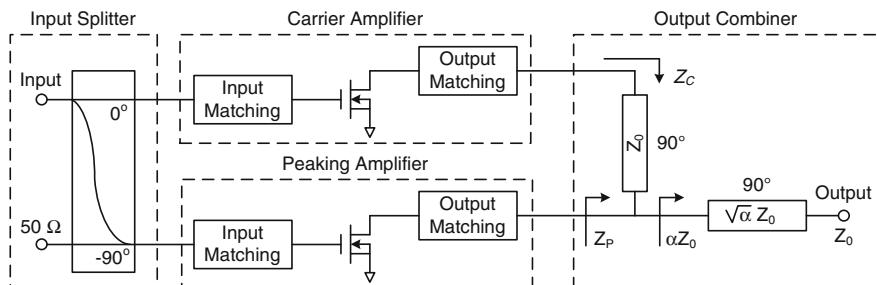


Fig. 2.9 Block diagram of the standard Doherty PA

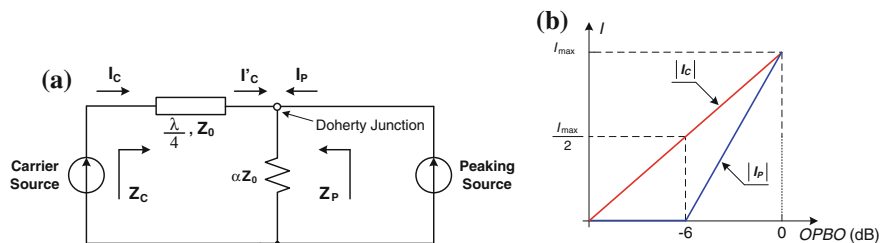
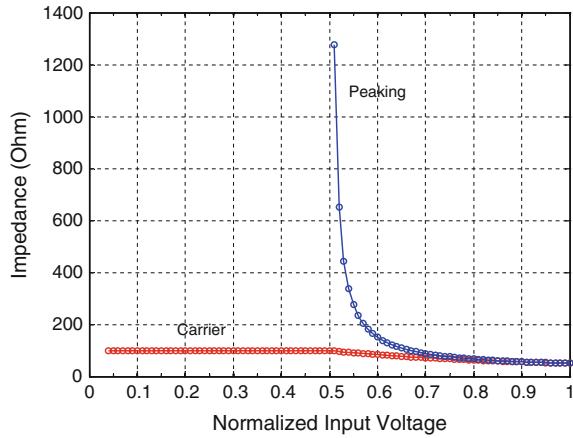


Fig. 2.10 **a** Equivalent operational circuit of the Doherty PA; **b** Ideal output current profile

Fig. 2.11 Impedance seen by the Doherty amplifier



both carrier and peaking amplifiers are contributing to the output power of the Doherty PA.

At low input power levels, the peaking amplifier is turned *off*, and its branch ideally presents an open circuit. As inferred from Fig. 2.11, because of the action of the impedance inverter, the carrier amplifier will be operating into a load, Z_C , given by

$$Z_C = \frac{(Z_0)^2}{\alpha Z_0} = \frac{Z_0}{\alpha} \quad (2.7)$$

where Z_0 is the output load of the Doherty PA, which is usually equal to 50 Ω .

The load impedance of the carrier amplifier remains unchanged as long as the peaking amplifier is still turned *off*. This causes the premature saturation of the carrier amplifier at $20\log_{10}(\alpha)$ dB back-off from the Doherty PA-peak power level, which leads to an efficiency maximum at this power level.

As soon as the input power goes beyond the conduction threshold of the peaking amplifier, the latter starts contributing to the total output power of the Doherty PA. This creates an active load modulation mechanism; and, as illustrated in Fig. 2.11 (for $\alpha = 0.5$ and $Z_0 = 50 \Omega$), the load impedance of the carrier amplifier decreases gradually from its value given by (2.7) to Z_0 , and that of the peaking amplifier, Z_P , drops rapidly from a very large value (theoretically infinite, ∞) to Z_0 . In this case, an efficiency maximum occurs at peak power drive.

2.4.2 Efficiency Calculation and Optimization of Doherty Amplifier

The theoretical efficiency of a Doherty PA, the carrier and peaking amplifiers of which are operating in class B, is given by Ebrahimi et al. [1]

$$\eta(\text{OPBO}, \alpha) = \begin{cases} \frac{\pi}{4} \cdot \frac{1}{\alpha} \cdot 10^{\frac{\text{OPBO}}{20}}, & \text{OPBO} \leq 20\log_{10}(\alpha) \\ \frac{\pi}{4} \cdot \left(\frac{10^{\frac{\text{OPBO}}{20}}}{(1+\alpha) \cdot 10^{\frac{\text{OPBO}}{20} - \alpha}} \right), & 20\log_{10}(\alpha) \leq \text{OPBO} \leq 0 \end{cases}, \quad (2.8)$$

where output power back-off (OPBO) refers to the back-off of the actual output power of the Doherty PA from its saturation power.

Figure 2.12 depicts the simulated efficiency as a function of OPBO for various values of α . It is clear that the active load modulation mechanism allows the maintenance of a relatively high efficiency over the power range $P_{\text{sat,dB}} - 20\log_{10}(\alpha)$ to $P_{\text{sat,dB}}$, where $P_{\text{sat,dB}}$ is the output saturation power, expressed in dB, of the Doherty PA. Furthermore, it can be seen that the choice of α shapes the efficiency curve of the Doherty PA. A typical choice for the Doherty design parameter is $\alpha = 0.5$, which, by definition, means that the carrier and peaking amplifiers should contribute equally to the peak output power. Symmetrical Doherty PA commonly denotes this specific type.

In practice, the design of Doherty PAs for optimal performance should consider the operating conditions at high- and low-power regions.

At peak power condition, the carrier and peaking amplifiers are ideally operating into 50Ω . The design of the single-ended carrier and peaking amplifiers consists of determining the appropriate source and load impedances and designing the input and output matching networks that are required to achieve the targeted performance in terms of power efficiency or output power. The design procedure is well established and a load-pull-based approach is often adopted.

Fig. 2.12 Theoretical efficiency of the Doherty PA

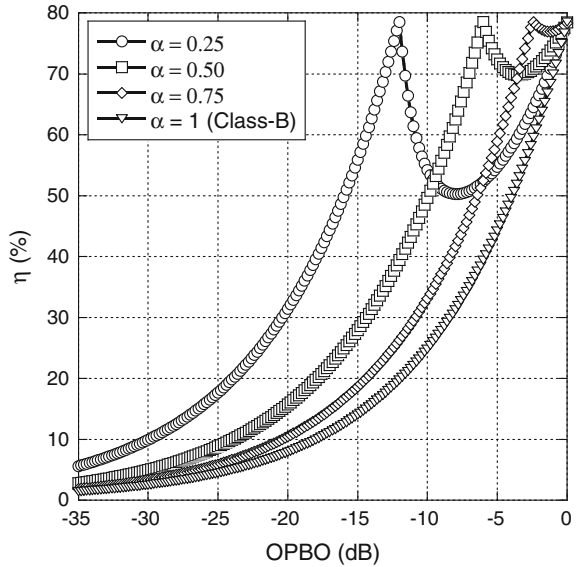


Fig. 2.13 Doherty PA design optimization in the peaking branch

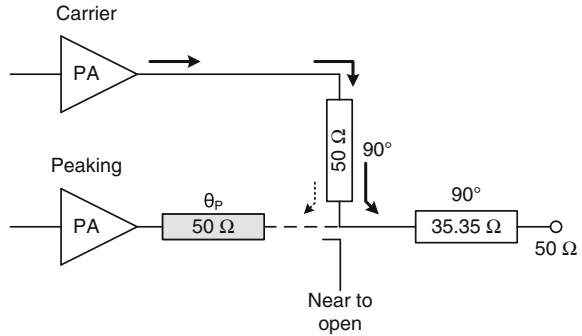
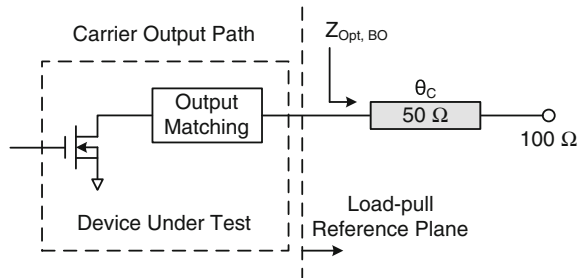


Fig. 2.14 Doherty PA design optimization in the carrier branch



At the low-power region, the design considerations of the carrier and peaking amplifiers are different. First, the peaking branch should present an open circuit to prevent the leak of output power from the carrier amplifier into the peaking path when the peaking amplifier is still turned *off*. As depicted in Fig. 2.13, this problem can be surmounted by inserting an offset line (θ_p) following the peaking amplifier to ensure the quasi-open-circuit condition.

Second, the performance of the carrier amplifier at back-off (i.e., when the peaking amplifier is still inactive) should be optimized as it will dominate the overall performance of the Doherty PA when driven with modulated signals with high PAPRs. As illustrated in Fig. 2.14, this can be achieved by means of a series offset line (θ_c) that converts the 100 Ω seen by the carrier amplifier at back-off to an optimal matching point, $Z_{\text{Opt,BO}}$, that gives the best possible performance around the turn-on point of the peaking device. Detailed explanations related to design optimization of dual-branch Doherty PAs are discussed in [2].

2.5 Pulsed-Load-Modulated Amplifier

The pulsed-load-modulated (PLM) PA was first introduced in 2010 [3]. This technique benefits from the delta-sigma envelope modulation at the gate supply of the power amplifier to dynamically modulate the load at the output of the PA to improve

the power efficiency performance. Delta-sigma modulation (DSM) technique is explained in Sect. 2.7. Unlike Doherty PA, in the PLM PA, the dynamic load variation is dependent on the duty cycle of the DSM signal and it will be shown that the and the average efficiency of the ideal PLM amplifier stays at its maximum value for up to 6 dB back-off from the peak output power [4]. This section will survey the concept of the dynamic load modulation in PLM power amplifiers and its effect on their power efficiency performance.

2.5.1 Load Modulation in Switched Resonators

Digital load modulation of the PLM amplifier is based on dynamic load variations in switched resonator circuit. Figure 2.15 shows a typical switched resonator circuit with a series LC tank. A switched resonator consists of a switched controlled RF source, a high Q resonator [or band-pass filter (BPF)] tuned at the frequency of the RF input signal, terminated with a load.

The energy stored in the resonator is controlled by the switching action speed so that variable and duty-cycle dependent impedance behavior can be obtained at the input of the resonator. If the switching action happens with a switching period (T) shorter than the time constant of the resonator and with a switching frequency less than the RF signal frequency (f_c), the on-state voltage at the output of the resonator, V_{out} can be approximated by the product of the duty cycle, D , and the voltage at the input of the switched amplifier, V_A is as follows:

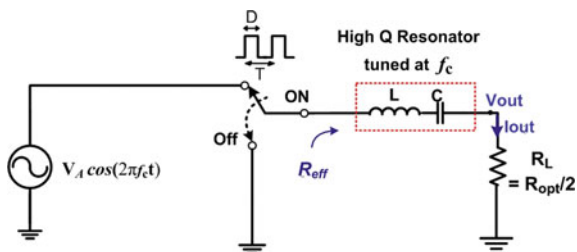
$$V_{out} = DV_A \quad (2.9)$$

The current at the output of the resonator, I_{out} is about the same as the one at its input and it can be approximated by the following equations:

$$I_{out} = \frac{V_{out}}{(R_{opt}/2)} = \frac{2DV_{max}}{(V_{max}/I_{max})} = 2DI_{max} \quad (2.10)$$

where $R_{opt} = \frac{V_{max}}{I_{max}}$ is the optimum matching impedance of the class-B amplifier. In this equation, V_{max} and I_{max} are the maximum voltage and current of the class-B amplifier.

Fig. 2.15 Block diagram of a switched resonator circuit with a series LC tank



Hereafter, we consider the switched amplifier is fully driven such that $V_A = V_{\max}$.

During the *off* state of the switched amplifier, the *off* state voltage is practically zero. Therefore, the effective resistance, R_{eff} , at the output of the switched amplifier can be approximated by the following:

$$R_{\text{eff}} = \begin{cases} \frac{V_A}{I_{\text{out}}} = \frac{(V_{\text{out}}/D)}{I_{\text{out}}} = \frac{1}{D} \cdot R_L = \frac{1}{D} \cdot R_{\text{opt}}/2 & 0 \leq t < D \cdot T \\ 0 & D \cdot T \leq t < T \end{cases} \quad (2.11)$$

From Eq. (2.11), one can conclude the effective output resistance of the switched amplifier increases from $R_{\text{opt}}/2$ to infinity when the duty cycle varies from 100 to 0 %.

The output power at the load can be calculated as:

$$P_{\text{out}} = \frac{1}{2} I_{\text{out}} V_{\text{out}} = \frac{1}{2} \left(\frac{DV_A}{R_{\text{out}}/2} \right) (DV_A) = V_{\text{max}}^2 \frac{D^2}{R_{\text{opt}}} = D^2 V_{\text{max}} I_{\text{max}} \quad (2.12)$$

From these equations, it can be seen that in a switched resonator circuit, the load impedance at the input of the resonator and the output power can be controlled by the duty cycles of the switching pulses. This dynamic load variation is very beneficial in designing high efficiency PAs since the optimal efficiency in the amplifier can be achieved when the load impedance is inversely proportional to the square root of the output power.

2.5.2 PAs with Pulsed-Load Modulation

Figure 2.16 shows a simple block diagram of a PLM power amplifier. As can be seen in this figure, in the PLM amplifier structure, the main and auxiliary amplifiers are connected together by a 90° transmission line and they are switched at the same time by the modulated envelope of the signal between the class B (the *on* state) and pinch-off (the *off* state). Using digital signal processing techniques such as pulsed width modulation (PWM) or DSM, the time envelope varying signals can be converted to constant envelope signals. The constant envelope modulated signal is then transmitted to the gate biases of the main and auxiliary amplifiers. The phase of the signal is up-converted to the carrier frequency and is then fed to the input of the amplifier. In order to remove the quantization noise caused by the envelope modulator from the output signal, a band-pass filter (BPF) with a high quality factor is placed at the output of the power amplifier.

The efficiency enhancement method in the PLM PA is derived from the mechanism of the load modulation in series with LC switched resonators. If the switching action at the gates of the main and auxiliary amplifiers occurs faster than the bandwidth of the output filter, the effective input impedance of the filter (R_{eff})

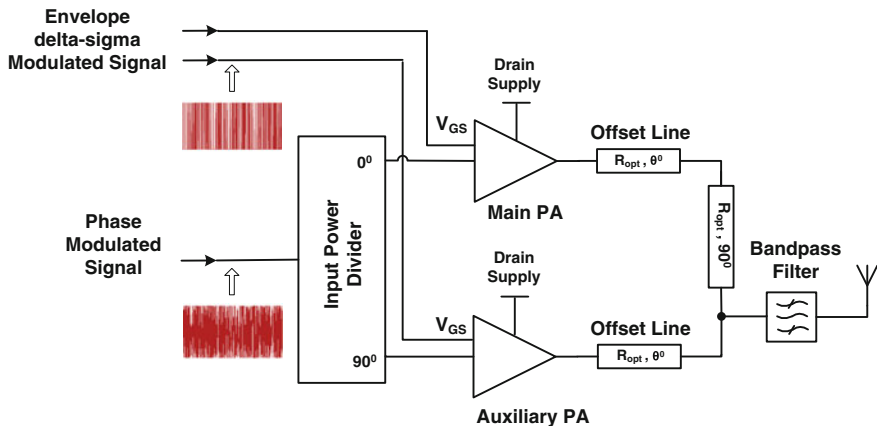


Fig. 2.16 A simple block diagram of the PLM power amplifier

varies inversely with the duty cycle of the gate bias pulses. Consequently, it can be shown that the output power is proportional to the square of the duty cycle of the switching pulses during the *on* state, and the optimal efficiency performance can be achieved.

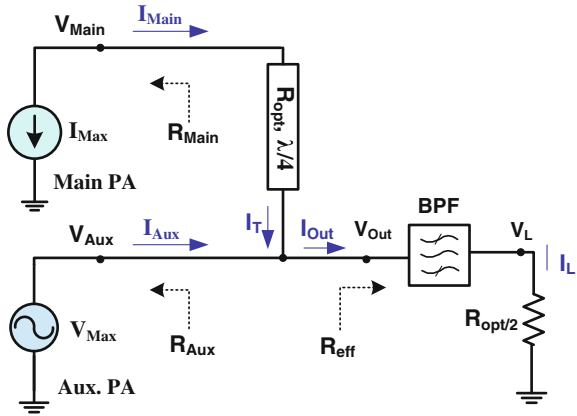
When the gate pulses are *off*, both transistors are turned *off* simultaneously. The $\lambda/4$ transmission line is used at the output of the main amplifier to transfer the main PA high-output impedance to a virtual ground at the input of the BPF. Therefore, as in series LC switched resonators, there is a short circuit at the input of the filter and R_{eff} equals zero. During the high level of the gate pulses (*on* state), the auxiliary amplifier is forced to operate in the saturation mode due to the load modulation occurring at its output. Therefore, the auxiliary amplifier can be modeled as a voltage source during the *on* state such as in switched resonators.

In the design of the PLM PA, the main branch has slightly higher voltage than the auxiliary PA branch. Hence, for the low input power levels (when the gate pulse duty cycles are less than 50 %), the main amplifier provides most of the current to the output load. However, at high input power levels (when the duty cycle of the gate pulses are higher than 50 %), both main and auxiliary amplifiers conduct current to the load. Figure 2.17 depicts a simple model of the PA at the *on*-state level of the gate pulses.

The performance of the amplifier can be analyzed and tested using variable duty cycle pulses as gate biases for both main and auxiliary PAs.

Back-off mode of operation ($OPBO > 6$ dB) For pulses with duty cycles less than 50 %, the OPBO level is more than 6 dB. In this region, the main amplifier provides most of the current to the output load terminal. At OPBO levels greater than 6 dB or for duty cycles less than 50 %, according to (2.10) the output current at the combination point can be expressed as follows

Fig. 2.17 Equivalent circuit of the PLM amplifier at high-level gate pulses



$$I_T = I_{out} = 2DI_{max} \quad (2.13)$$

Hence the output current and voltage of the main amplifier are

$$I_{Main} = jI_{max} \quad (2.14)$$

$$V_{Main} = jR_{opt}I_T = jR_{opt}(2DI_{max}) = 2jDV_{max} \quad (2.15)$$

and the load impedance seen by the main amplifier is given by

$$R_{Main} = \frac{V_{Main}}{I_{Main}} = 2DR_{opt} \quad (2.16)$$

Since the auxiliary amplifier is modeled as voltage source having amplitude of V_{max} and according to (2.11), it is loaded with relatively high impedance; therefore almost no current is generated from it. The current and voltage at the output of the auxiliary amplifier are $I_{Aux} = 0$ and $V_{Aux} = V_{max}$.

Consequently, using (2.12) and assuming class B mode of operation for the main amplifier, the drain efficiency of the PLM amplifier can be calculated as follows:

$$\begin{aligned} \eta_{PA} &= \frac{P_{out}}{P_{DC}} = \frac{D^2 I_{max} V_{max}}{I_{DC-Main} V_{DC-Main}} = \frac{D^2 I_{max} V_{max}}{(I_{max}/\pi)(2DV_{max})} = \frac{D^2 I_{max} V_{max}}{(\frac{2}{\pi} DI_{max})(V_{max})} \\ &= \frac{\pi D}{2}, \quad 0 < D < 50\%. \end{aligned} \quad (2.17)$$

Back-off mode of operation ($0 \text{ dB} < \text{OPBO} < 6 \text{ dB}$) As the duty cycle of the gate pulses increases from 50 to 100 %, entering the 6 dB OPBO region, the main

amplifier provides I_{\max} to the output load, and the auxiliary amplifier starts providing the remaining current to the load as its output impedance reduces because of the load modulation behavior of the PLM power amplifier. At the full power level, both amplifiers contribute equally in delivering the maximum combined current of $2I_{\max}$ to the load, $R_{\text{opt}}/2$. At less than 6 dB OPBO, considering (2.10), the currents in the main and auxiliary are as follows:

$$I_T = I_{\max}, \quad I_{\text{Aux}} = I_{\text{out}} - I_T = (2D - 1)I_{\max} \quad (2.18)$$

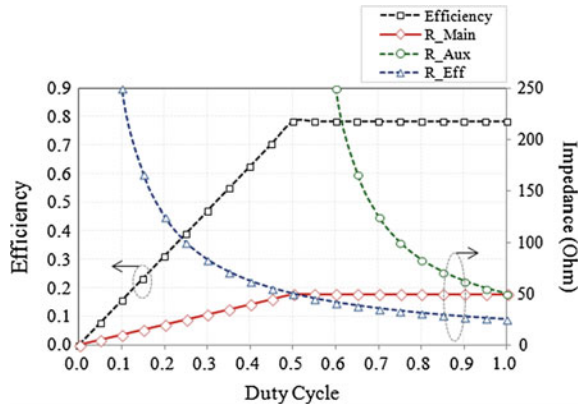
$$I_{\text{Main}} = jI_{\max}, \quad V_{\text{Main}} = jR_{\text{opt}}I_T = jV_{\max}. \quad (2.19)$$

Using (2.12), the drain efficiency of the PLM amplifier in the 6 dB OPBO region can be calculated as

$$\begin{aligned} \eta_{PA} &= \frac{D^2 I_{\max} V_{\max}}{I_{DC-\text{Main}} V_{DC-\text{Main}} + I_{DC-\text{Aux}} V_{DC-\text{Aux}}} \\ &= \frac{D^2 I_{\max} V_{\max}}{\left(\frac{1}{\pi}\right)[I_{\max} + (2D - 1)I_{\max}]2DV_{\max}} = \frac{\pi}{4}, \quad 50 \leq D \leq 100\% \end{aligned} \quad (2.20)$$

Since both amplifiers stay in saturation at 6 dB OPBO region, the efficiency of the PLM PA stays at the optimum value (around 78 % for ideal class-B amplifiers). Figure 2.18 shows the ideal drain efficiency of the PA along with the load impedances seen at the output of the main and auxiliary amplifiers R_{Main} and R_{Aux} for different duty cycle values. In this analysis, the optimum load impedance of the main and auxiliary amplifiers R_{opt} is supposed to be 50Ω . It can be seen in this figure that the load impedance R_{eff} varies inversely with the duty cycle values.

Fig. 2.18 Theoretical drain efficiency of the PA and the load impedances seen at the output of the main and auxiliary amplifiers (R_{Main} and R_{Aux}) for variable duty cycles



2.6 Linc Amplifiers

2.6.1 LINC Amplifier Architecture

The LINC amplifier is a two-branch amplifier, illustrated in Fig. 2.19.

The principle of operation of the LINC amplifier is based on converting the varying-envelope input signal, $S_{in}(t)$, into two constant envelop- and phase-modulated signals $S_1(t)$ and $S_2(t)$, which can be obtained using the following expression:

$$S_{in}(t) = r(t) \cdot e^{j\phi(t)} = S_1(t) + S_2(t) \quad (2.21)$$

where $r(t)$ is the envelop of the input baseband signal and $\phi(t)$ is its phase.

By writing the envelop of the signal as

$$r(t) = r_{\max} \cdot \cos(\theta(t)) \quad (2.22)$$

With $r_{\max} = \max(|s_{in}(t)|) = \max(r(t))$ and $\theta(t) = [\cos(r(t)/r_{\max})]^{-1}$.

One can deduce using the two equations above that the phase-modulated signals after signal decomposition are

$$\begin{cases} S_1(t) = \frac{r_{\max}}{2} \cdot e^{j(\phi(t) + \theta(t))} \\ S_2(t) = \frac{r_{\max}}{2} \cdot e^{j(\phi(t) - \theta(t))} \end{cases} \quad (2.23)$$

The resultant signal, $S_{out}(t)$, at the output of the amplifier, having voltage gain, G , is a linearly amplified version of the input signal $S_{in}(t)$:

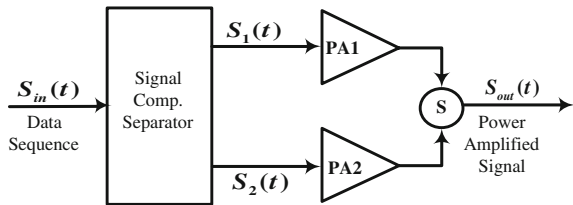
$$S_{out}(t) = G \cdot S_{in}(t) \quad (2.24)$$

Another way to compute $S_1(t)$ and $S_2(t)$ using geometrical reasoning is illustrated in Fig. 2.20:

$$\begin{cases} S_1(t) = \frac{1}{2}S(t)[1 + j \cdot e(t)] \\ S_2(t) = \frac{1}{2}S(t)[1 - j \cdot e(t)] \end{cases} \quad (2.25)$$

where $e(t) = \sqrt{\frac{r_{\max}^2}{r^2(t)} - 1}$

Fig. 2.19 LINC amplifier block diagram



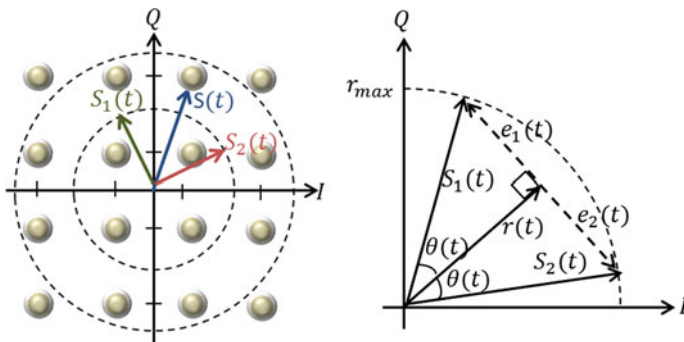


Fig. 2.20 LINC vector decomposition

Considering that $S_1(t)$ and $S_2(t)$ have constant envelopes, they can be efficiently amplified by means of power-efficient or saturated or switching-mode PAs. The two amplified signals are then combined to retrieve a linearly amplified replica of the original amplitude-modulated input signal. Therefore, the RF PAs can be operated at saturation, to achieve maximum power efficiency. The structure of a LINC amplification system is shown in Fig. 2.21. A vector representation of the separated baseband components is also given in Fig. 2.20. There are three main components in the LINC transmitter, which are the signal separator, the nonlinear amplifiers, and the signal combiner [5]. A brief discussion of each block is covered as follows.

A successful implementation of a LINC transmitter is highly dependent on the precision and control of signal separation, because the LINC architecture is sensitive to amplitude and phase balance [5].

The PAs should be designed for the highest possible efficiency at saturation, based on the selection of the biasing and impedance matching circuits. For this reason, class-F and inverse class-F PA designs that have high power efficiencies can be used. The bandwidth response of the PA needs to be carefully selected, as the LINC-separated signals have larger bandwidth than the original envelope modulated signal, because of added phase modulation. Additionally, the power-amplification

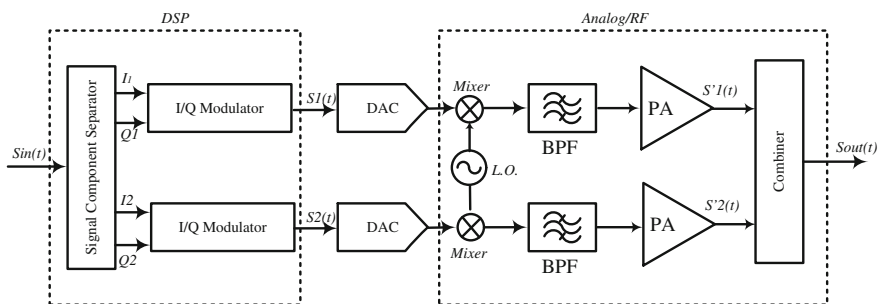


Fig. 2.21 LINC transmitter structure

block should be made of two identical or quasi-identical amplifiers in order to preserve amplitude and phase balance between two branches [5].

The use of two highly efficient PAs operated with constant envelope signals in the LINC system does not guarantee that the overall efficiency of the LINC transmitter will be high, but the available power at the output of the combiner will determine the transmitter's overall efficiency. The average efficiency of the LINC system depends also on the power distribution function (PDF) of signal and the type of combiner used. Hence, the combining structure is a key factor in the overall power efficiency as well as the linearity of the LINC transmitter.

Two possible combining structures can be used: (i) the matched and isolated combiner, and (ii) the nonmatched and nonisolated combiners that are also referred in the literature as outphasing or Chireix combiners [5]. The overall system efficiency of the LINC amplifier, η_{LINC} , is given by

$$\eta_{\text{LINC}} = \eta_{\text{PA}}^{\text{Peak}} \cdot \eta_c \quad (2.26)$$

where $\eta_{\text{PA}}^{\text{Peak}}$ is the peak amplifier efficiency, and η_c is the system-combining efficiency.

2.6.2 Case of Matched and Isolated Combiner

In the case of a matched and isolated combiner shown in Fig. 2.22, the system instantaneous combining efficiency can be calculated as follows:

$$\eta_c(t) = \frac{P_{\text{out}}}{P_1 + P_2} = \frac{1}{2} \frac{|S_{\text{out}}|^2}{G^2 (|s_1|^2 + |s_2|^2)} = \frac{|s_{\text{in}}|^2}{r_{\text{max}}^2} = \cos^2(\theta(t)) \quad (2.27)$$

The system-combining efficiency reaches its maximum (unity) at peak power and drops fast as the signal drive level decreases. This equation concludes that despite the branch amplifier has very high efficiency, the LINC amplifier efficiency drops rapidly at low-level signals as low as $\eta_{\text{PA}}^{\text{Peak}}/10$, at power back-off operation of 10 dB.

Fig. 2.22 The Wilkinson combiner

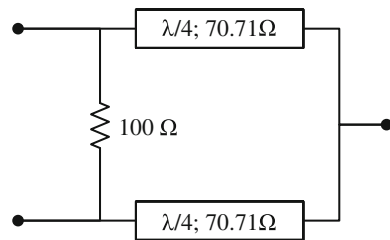


Figure 2.23 shows the comparative efficiency performance of the LINC system using isolated (Wilkinson) combiner against class-B amplifier:

The average efficiency of the LINC amplifier depends on the signal's PDF. If the latter is known analytically, one can compute the average LINC efficiency by:

$$\eta_{\text{Avg}} = \eta_{\text{PA}}^{\text{Peak}} \int_0^{\pi/2} p(\theta) \cos^2(\theta) d\theta \quad (2.28)$$

where $\eta_{\text{PA}}^{\text{Peak}}$ is the peak efficiency of each RF amplifier branch, and $p(\theta)$ is the PDF of signal at $\theta(t)$.

Figure 2.24 illustrates how the average combining efficiency depends on the signal statistics. It is clear that the average combining efficiency for the orthogonal frequency division multiplexing (OFDM) signal will be about 65 % and that of CDMA signal will be about 50 %.

As for the linearity, the LINC system with hybrid combiner is assumed to occur with high linearity if the two branches are perfectly balanced and the combiner does not introduce any imbalance in phase or amplitude between two branches.

Fig. 2.23 Efficiency of the LINC system using the Wilkinson combiner and class-B amplifier

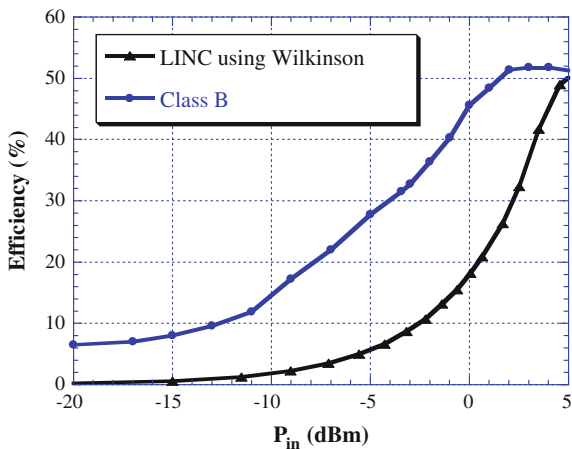
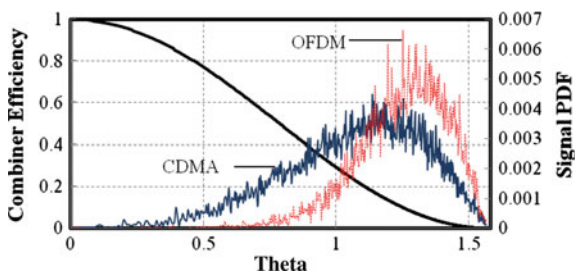


Fig. 2.24 Average efficiency of the LINC amplifier for CDMA and OFDM signals

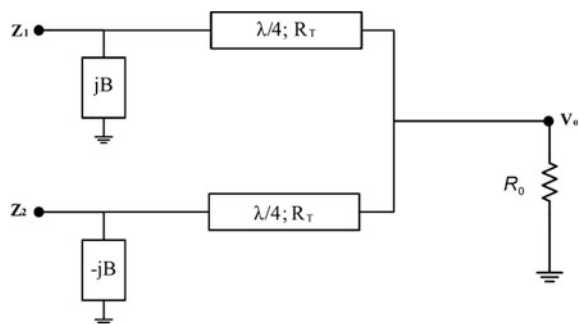


2.6.3 Case of Nonmatched Combiners (Chireix Combiners)

This second class of combining structures groups the unmatched lossless outphasing combiners. This class includes the lossless Wilkinson-type combiner, i.e., without the isolation resistor, and a combiner that typically includes two quarter-wavelength transmission lines, a tee junction, and shunt reactance of opposite values at the input of each transmission line, which is typically called the Chireix-outphasing combiner. Figure 2.25 shows the Chireix-outphasing combiner structure with Z_c representing the characteristic impedance of the quarter-wavelength transmission line, and B is the magnitude of the susceptance of the shunt elements in the combiner, which are named stubs. This susceptance is added to improve efficiency by canceling the imaginary part of load presented to the RF amplifier at a certain power back-off. Z_o is the impedance of the output load, and V_o is the output voltage. Branch 1 of this combiner amplifies the $+\theta(t)$ phase signal and has a shunt element with $+B$ susceptance. Branch 2 of the combiner amplifies the $-\theta(t)$ phase signal and has a shunt element with $-B$ susceptance.

The Chireix combiner or lossless combiner can be presented as a very good solution to the problem of degradation of efficiency observed when the matched combiner is used. The Chireix combiner as described above does not have an isolated port load to dissipate any energy. Consequently, the nonisolating combiner presents time-varying impedances to the output of the RF amplifier of each branch as the phase difference between the branches increases, thus improving the LINC average efficiency significantly. To describe the behavior of load impedance variation, Raab [6] gives the expression for time-varying impedance/admittance and its impact on the efficiency of several kinds of power amplifiers. In [7], Stengel found similar results on the combiner efficiency and optimization using a different approach and ideal voltage sources. Assuming that the RF amplifiers exhibit ideal voltage source behavior, the DC-power consumption will scale according to the load impedance, i.e., the efficiency remains high regardless of the phase difference between branches. For an ideal voltage source, its output voltage is not affected by its output current. The voltage magnitude remains fixed, and the voltage phase is only modulated by the phase of the control signal. Thus, the constant envelope

Fig. 2.25 The Chireix-outphasing combiner



signal principle at each branch is kept, and the internal impedance of RF amplifier of each branch is considered equal to zero. Using the topology of the Chireix combiner depicted in Fig. 2.25, where the shunt susceptance B is introduced to improve the LINC system average efficiency, the resulting formula of the impedance variation found in [7] is modified to introduce the R_o impact, as follows:

$$Z_{1,2} = \left[\left(\frac{2R_o}{R_T^2} \right) (\cos^2(\theta(t)) \pm j(B' + \sin(2\theta(t)))) \right]^{-1} \quad (2.29)$$

with $B' = \frac{BR_o^2}{2R_T}$

Figure 2.26 shows how the instantaneous efficiency changes as a function of the power back-off for given values of B' , directly related to the value of shunt susceptance, B , assuming that R_o and R_T are fixed by the design of the power combiner.

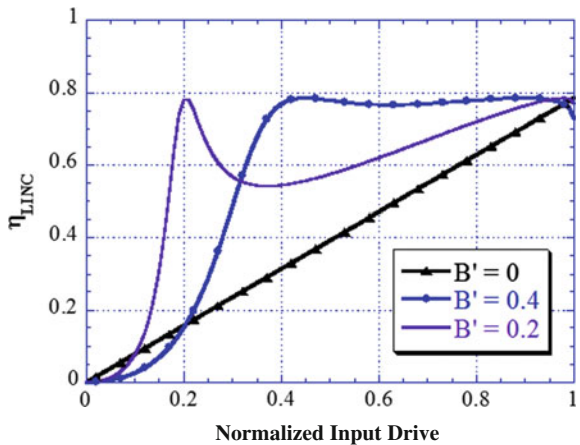
In the Chireix combiner, the parallel admittance B is introduced to improve the LINC average efficiency. In this case, the average efficiency can be expressed as

$$\eta_{\text{Avg}}^{\text{Chireix}} = \eta_{\text{PA}}^{\text{Peak}} \int_0^{\pi/2} p(\theta) \eta_c^{\text{Chireix}}(\theta) d\theta \quad (2.30)$$

where $\eta_c^{\text{Chireix}}(\theta)$ is the instantaneous combiner efficiency that can be obtained, as follows [6]:

$$\eta_c^{\text{Chireix}}(\theta) = \frac{\text{real}(Z_{1,2})}{\text{mag}(Z_{1,2})} \quad (2.31)$$

Fig. 2.26 Efficiency of the LINC amplifier



The parallel admittance B allows the designer to maximize the instantaneous efficiency of combiner η_{Comb} . By choosing the value of B when the imaginary part of $Z_{1,2}$ is equal to zero, the instantaneous efficiency η_{Comb} is maximized for a certain value θ_m of θ . To optimize the average efficiency of the Chireix combiner, the designer needs to define the type of modulation used in the LINC system and use the PDF of the signal to obtain the optimum value θ_m of θ , which gives the maximum of the expression (2.31). If this is done, then the value of admittance B can be fixed. Indeed, the Chireix system presents an important improvement in efficiency compared to the LINC using the hybrid combiner. As noted above, this improvement in efficiency is obtained at the cost of degradation of linearity.

2.7 Delta-Sigma-Based Transmitters

A power amplifier (PA) operation in Class AB or in Class B outputs its maximum efficiency while it is driven by its maximum allowable input. For high throughput modulation signals, for example quadrature amplitude modulations (QAMs) such as 16-QAM and 64-QAM modulated, the envelope is varying and the peak power of the signal occurs at very short periods. Hence, the PA could not be driven to more than its saturation power, it should be driven at the back-off from its peak input power. This power difference is a property of the signal is defined as the peak to average ratio PAPR.

2.7.1 Delta-Sigma Modulation

A delta-sigma modulator as illustrated in Fig. 2.27c is able to shape the envelope varying signal, illustrated in Fig. 2.27a into a constant envelope pulse train signal illustrated in Fig. 2.27b, in such way the information is coded in the phase and the amplitude of the input signal will be converted to the pulse's width and pulse's separation information at the output of the sigma delta modulator (DSM). In this case, The PA fed by a DSM signal could work at its maximum efficiency without need to any power back-off. A high efficiency switching-mode PA (SMPA) placed at the output of the DSM could be used without causing a distortion to the delta-sigma modulated signal providing that an RF BPF is placed at the output of the PA. The DSM is based on oversampling and quantizing a baseband time-varying envelope signal and encode it to a bi-level constant envelope signal. A feedback signal in the DSM contains the quantized signal is subtracted from the input signal. A block diagram shows the building blocks of the DSM. At first, as illustrated in Fig. 2.27c, the input signal is subtracted from the feedback quantized signal to extract the quantization noise. Then, this quantization noise is filtered out and pushed away from the signal channel using filter with bandwidth equal to the input signal bandwidth [7] (Fig. 2.27).

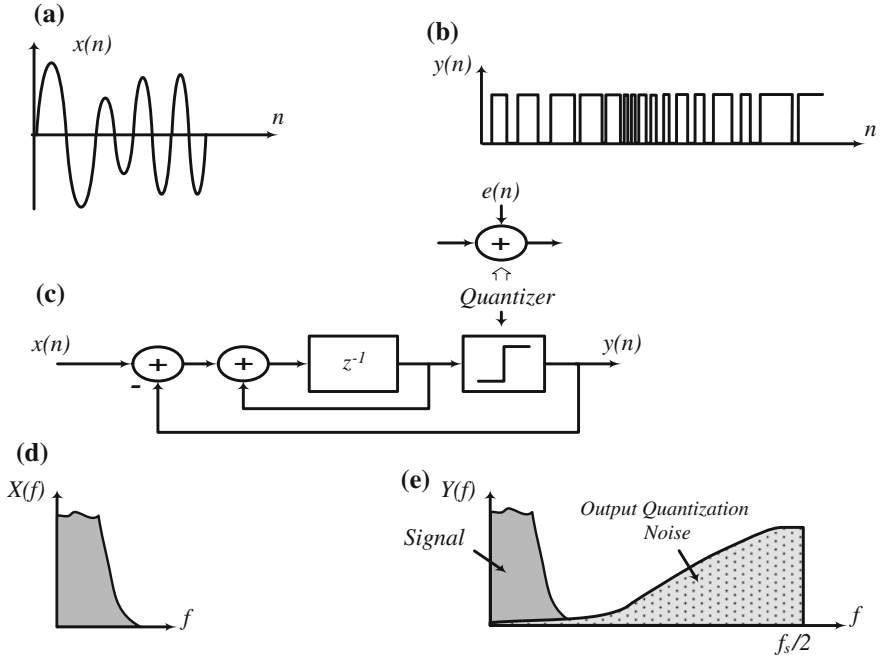


Fig. 2.27 First order delta-sigma modulator

The low-pass transfer function of the first-order DSM given in Eq. (2.1a) shows that the signal and quantization noise pass through different transfer functions; the signal transfer function STF and the noise transfer function NTF

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \quad (2.32)$$

With $\text{STF} = z^{-1}$ and $\text{NTF} = (1 - z^{-1})$.

The two important parameters for a DSM which reduce and shape the quantization noise are the order of the modulator and the over sampling rate defined by

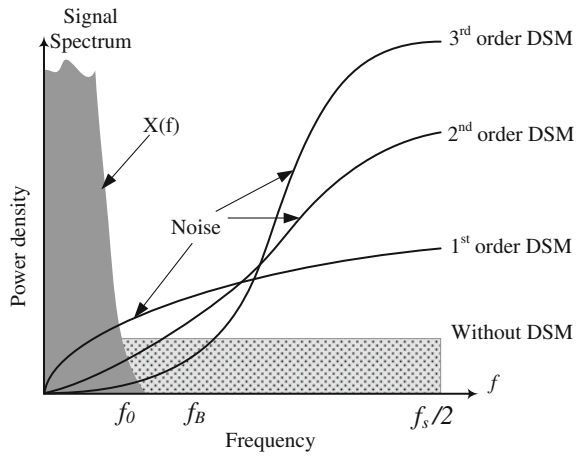
$$\text{OSR} = \frac{f_s}{\text{BW}}, \quad (2.33)$$

where f_s is the sampling frequency and BW is the bandwidth of the input signal.

In DSM the quantization and noise is distributed over $-f_s/2$ to $+f_s/2$; by increasing the OSR, the quantization noise is spread further and its level is lowered. By increasing the order of the modulator, the quantization noise shaping results in better noise rejection as shown in Fig. 2.28.

Modulators with higher order such as the third-order perform a higher order difference operation of the error produced by the quantizer and thus stronger attenuation at low frequencies for the quantization noise signal. The baseband

Fig. 2.28 Noise transfer function for different DSM orders



quantization error power for the third-order system is clearly smaller than for the first-order modulator as shown in Fig. 2.28. The increase of the order of the DSM improves the noise shaping but it is limited by some stability issues during actual implementation.

A block diagram of a second-order DSM is illustrated in Fig. 2.29

The transfer function of the second-order modulator is as follows:

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})^2 E(z) \quad (2.34)$$

The general block diagram of practical DSM modulator can be illustrated by Fig. 2.30.

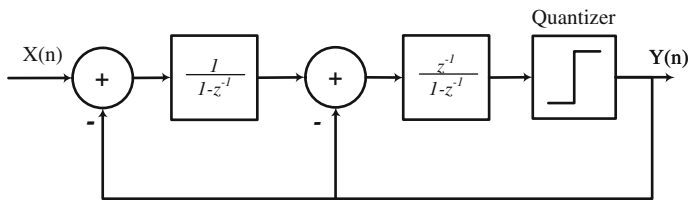
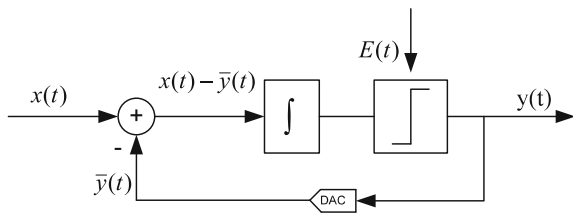


Fig. 2.29 Second order delta-sigma modulator

Fig. 2.30 Generic functional block diagram of delta-sigma modulator



2.7.2 DSM-Based Transmitter

There are three types of the DSMs classified according to the transfer function of the filter type: low-pass (LPDSM), band-pass (BPDSM) and high-pass (HPDSM).

Besides the low-pass LPDSM, two other delta-sigma topologies, BPDSM and HPDSM are used for delta-sigma-based transmitters. Unlike the LPDSM, the signal at the input of the BPDSM and the HPDSM should not be a baseband signal, but rather a signal at the IF or RF frequency, where low frequency noise does not degrade the signal quality.

The BPDSM and the HPDSM transfer functions are easily found by replacing z^{-1} in the LPDSM's transfer function depicted by (1) with $-z^{-2}$ and $-z^{-1}$, respectively.

The output of the DSMs for the LPDSM, BPDSM and HPDSM configurations are located at frequencies of zero, $f_s/4$ and $f_s/2$,

Considering the modulator output frequency, different architectures can be used for the DSM transmitter: direct-conversion architecture for LPDSM and low-IF architecture for BPDSM and HPDSM [8].

Delta-sigma-based transmitter offers, in principle, some advantages such as linearity and PA efficiency, it suffers from few drawbacks. A major drawback is the need for a high clock speed to oversample the data to achieve good signal quality by distributing the same amount of the quantization noise over larger frequency band and consequently achieve smaller in-band noise. To overcome this limitation, parallel processing is often adopted, where parallel DSM branches work simultaneously at a lower speed to provide the same performance as the original DSM.

Figure 2.31 illustrates a typical delta-sigma-based transmitter that includes the DM modulator, a frequency up-converter, a saturated or switching-mode amplifier and RF BPF.

The main parameters of the DSM modulator are the coding efficiency of the baseband encoder (DS modulator), C_{eff} and the signal to noise and distortion ratio (SNDR) illustrated in Fig. 2.32 and defined by the following equations:

$$C_{\text{eff}} = \frac{\text{Mean Power (inband signal)}}{\text{Mean Power (total signal)}} \quad (2.35)$$

$$\text{SNDR} = 10\log\left(\frac{\text{signal Power}}{\text{In-band Noise and Distortion power}}\right) \quad (2.36)$$

2.7.3 Efficiency Calculation of DSM Transmitter

The overall power efficiency of the DSM transmitter is product of the DSM modulator coding efficiency and the power amplifier modulated peak efficiency corrected by a factor related of the duty cycle statistics of the bit stream encoded signal.

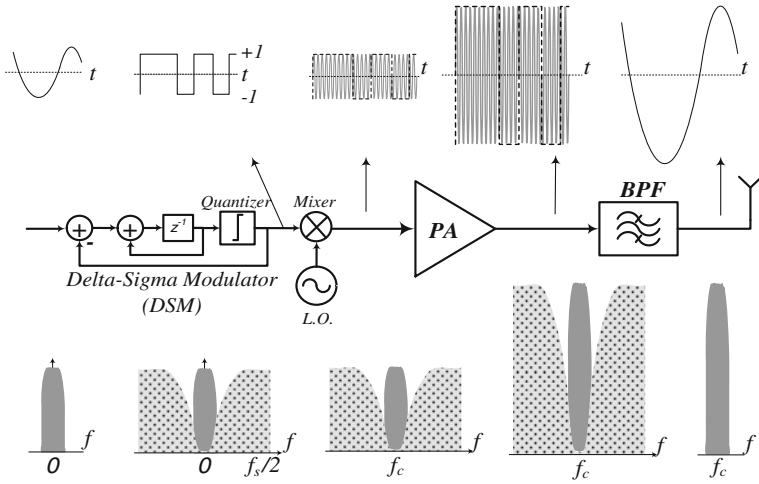


Fig. 2.31 Block diagram of DSM-based transmitter

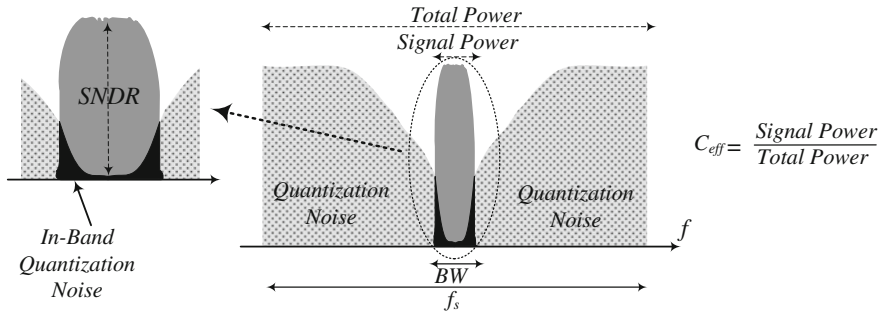


Fig. 2.32 SNDR and coding efficiency definition

The power amplifier modulated peak efficiency over the signal bandwidth, $\eta_{\text{PA_Peak}}^{\text{BW}}$, can be calculated as:

$$\eta_{\text{PA_Peak}}^{\text{BW}} = \frac{\int_{f_c - \text{BW}/2}^{f_c + \text{BW}/2} \text{PSD}(f) \eta_{\text{PA_Peak}}^{\text{CW}}(f) df}{\int_{f_c - \text{BW}/2}^{f_c + \text{BW}/2} \text{PSD}(f) df} \quad (2.37)$$

With f_c is the carrier frequency, PSD is power signal density of the signal at the output of the amplifier and BW is the bandwidth of the signal.

The bi-level signal at the output of the DS modulator, in most cases, does not have a 50 % duty cycle, which is a function of the signal bandwidth and its statistics. To compute the system average efficiency, the duty-cycle effect on the efficiency of the saturated or switching-mode PA has to be considered. Peak drain

efficiency, as a function of the duty cycle, can be defined for each PA class of operation as a parameter that accounts for the effect of the duty cycle on the average PA efficiency. Since different switching-mode PA classes respond differently to the variation of the duty cycle, duty-cycle effect on the efficiency calculation of DSM transmitters have to be taken into consideration when driven with different signals having different statistics. It has been demonstrated in [9] that class E amplifiers are the preeminent choice for efficient amplification purpose when driven with DSM signal.

The effect of the Duty cycle on the overall efficiency can be computed as follows:

$$\eta_{\text{Duty-cycle}} = \int_0^1 \text{PDF}_{\text{Duty-cycle}}(D) \eta_{\text{PA_Peak}}(D) dD \quad (2.38)$$

where D is the duty cycle, $\text{PDF}_{\text{duty-cycle}}(D)$ is the probability density function of the duty cycle of the signal and $\eta_{\text{PA-Peak}}(D)$ is the peak efficiency response of the switching-mode PA versus the duty cycle,

The overall average efficiency of the transmitter can be calculated as:

$$\eta_{\text{Average}} = C_{\text{eff}} \eta_{\text{PA_peak}}^{\text{BW}} \eta_{\text{Duty-cycle}} \quad (2.39)$$

It has been demonstrated in [9] that the effect in duty cycle on the LPDSM transmitter's efficiency is negligible and tends to unity.

For low-pass DSM transmitter using broadband PA, the average efficiency can be well approximated by the product of the coding efficiency and the peak efficiency of the PA as follows:

$$\eta_{\text{Average}} = C_{\text{eff}} \eta_{\text{PA_peak}} \quad (2.40)$$

2.7.4 Cartesian Delta-Sigma Transmitter

In this topology, the idea is to simply quantize both I and Q of the signal using two similar delta-sigma modulators. In that case, the I and Q information generate two quantized constant envelope signals and accordingly, the PA operates with the constant envelope signal to achieve the maximum efficiency. This architecture is very simple and easy to implement and is not sensitive to device linearity [1] (Fig. 2.33).

The output of the LPDSM is bi-level constant envelope signal which is directly up-converted by the IQ modulator. The output of the IQ modulator remains a constant envelope signal with four values of phases: $\pi/4$, $3\pi/4$, $5\pi/4$ and $7\pi/4$ while maintaining a constant envelope signal. The equation of the signals at the output of the IQ modulator is:

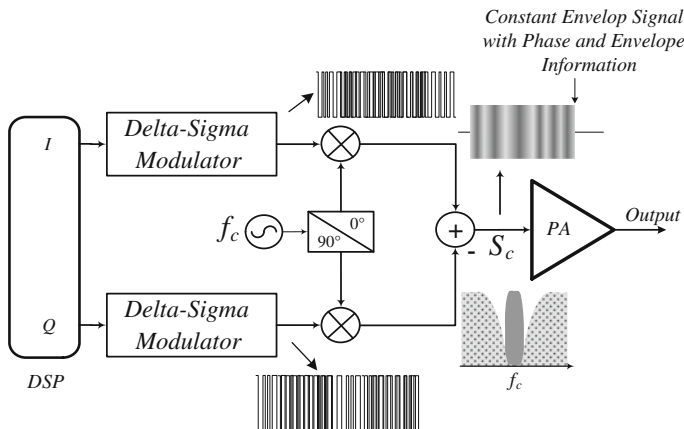


Fig. 2.33 Cartesian delta-sigma modulator

$$S_c = \sqrt{I^2 + Q^2} \cos\left(\omega_c t + \tan^{-1}\left(\frac{I}{Q}\right)\right) \quad (2.41)$$

$$|S_c| = \sqrt{I^2 + Q^2} = \sqrt{2} \quad (2.42)$$

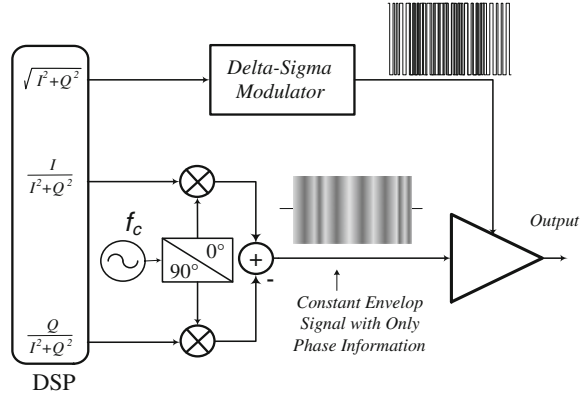
$$\angle S_c = \tan^{-1}\left(\frac{I}{Q}\right) = \frac{\pi}{4}, \frac{3\pi}{4}, \frac{5\pi}{4}, \frac{7\pi}{4} \quad (2.43)$$

2.7.5 Polar Delta-Sigma Transmitter

The polar DSM (PDSM) architecture is combined with the envelope elimination and reconstruction technique (EER) where the envelope of the signal is extracted from the signal and the constant envelope signal, which has only the phase information, is used to drive the SMPA. The envelope of the signal is restored back to the signal through the SMPA power supply. With a constant envelope input signal, the PA always operates at its saturation and accordingly, the efficiency of the PA and the transmitter is maximized [10] (Fig. 2.34).

The signal envelope in this technique is restored through modulation of the PA's power supply that works at its maximum efficiency. Consequently, a linear envelope modulation capability of the PA is necessary. In Cartesian DSM, I and Q components of the input signal are generated. Two DSM circuits are required to process the I and Q components, then the two quantized I and Q are summed together. It was shown that increasing the number of the quantization levels improves the coding efficiency of the DSM circuit [10]. In addition of the level quantization, the phase is also quantized to different four phase values.

Fig. 2.34 Polar delta-sigma modulator



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